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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/574,653	05/18/2000	Youngmin Kim	TI-29012	8503

7590 04/21/2004

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/574,653	KIM ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	AU

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 9-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 9-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Claims 1-3 and 9-12 are pending in the application. The 112-second-paragraph rejection to claim 1 is withdrawn.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Dawson et al. (US 5,963,803) in view of Wang et al. (US 6,020.231).

In re claims 1-3, Dawson et al., in Figs. 1A-1L and related text, expressly and inherently teach the claimed method of forming a CMOS sidewall spacer, comprising the steps of:

- forming a PMOS transistor gate structure 122 on a n-type region 108 of a semiconductor substrate 102 (Fig.1E);
- forming a NMOS transistor gate structure 126 on a p-type region 106 of said semiconductor substrate 102 (Fig.1E);
- forming initial single layer sidewall structure of similar widths adjacent to said NMOS gate structure 126 and said PMOS transistor gate structure 122, i.e. forming a silicon oxide layer covering said NMOS gate structure 126 and said PMOS transistor gate structure 122 (col. 6, lines 52-54); and

- anisotropically etching said initial single layer sidewall structure adjacent to said NMOS transistor gate structure 126 such that the width of a first single layer sidewall structure adjacent to said NMOS transistor gate structure (i.e. 144 having a thickness of **500** Å) is **less** than the width of a second single layer sidewall structure adjacent to said PMOS transistor gate structure (i.e. 146 having a thickness of **800** Å) (col.6, lines 61-67) .

In re claims 9-10 and 12, Dawson et al. also teach the claimed method of forming a CMOS sidewall spacer, comprising the steps of:

- providing a semiconductor substrate 102 of a first conductivity type such as p-type (col. 4, lines 63-64) with a region of a second conductivity type such as n-type region 108;
- forming a gate dielectric 112 on said semiconductor substrate 102;
- forming a conductive layer 114 on said gate dielectric 112 (Fig.1A);
- etching said conductive layer 114 and said gate dielectric 112 to form a first transistor gate stack (NMOS) with an upper surface on said semiconductor substrate 102 of a first conductivity (p-type) and a second transistor gate stack (PMOS) with an upper surface on said region of said semiconductor substrate of a second conductivity type (n-type, i.e. the N region 108) (Fig.1H);
- forming at least one single layer sidewall film (an oxide layer) over said semiconductor substrate 102 (col. 6, lines 47-54);
- anisotropically etching said single layer sidewall film (said oxide film) such that all of the sidewall film is removed from said upper surface of said first transistor gate stack

126 (NMOS) and said upper surface of said second transistor gate stack 122 (PMOS), wherein a plurality of single layer sidewall structure of a first width 146 are formed adjacent to said second transistor gate stack 122 (PMOS), and a plurality of single layer sidewall structure of a second width 144 are formed adjacent to said first transistor gate stack 144 (NMOS) (Fig.1H);

- masking said second transistor gate stack 122 with a photoresist pattern 148 used for source drain implantation (Fig. 1I); and
- etching said single layer sidewalls of said first width adjacent to said first transistor gate stack 126 (NMOS) thereby forming single layer sidewalls of a second width adjacent to said first transistor gate stack 126 (NMOS), wherein said second width 144 is **less** than said first width 146 (Fig.1H).

In re claim 11, Dawson et al. substantially teach the claimed method as stated above except utilizing plasma etch process as the anisotropically etching for forming the sidewalls at both sides of said PMOS and the NMOS transistors.

However, the plasma etch is a well-known practice for etching a sidewall film to form the sidewalls of a CMOS device, as evidenced by Wang et al., in which they states that " a conventional fabrication technique for forming such side wall spacer is by way of CVD forming of an oxide layer, and a subsequent step of anisotropic etching, typically either reactive ion etching or plasma etching." (col. 1, lines 40-43).

Therefore, it would have been obvious to one of the ordinary skill in the art at the time the invention was made to use the plasma etch as taught by Wang et al. to anisotropically etch the sidewall film of Dawson et al. for the purpose of forming sidewall structure of said PMOS

and said NMOS transistors since said plasma etch is a reliable method for selectively etching sidewall film with good dimension control. (col. 1, lines 40-43, Wang et al.).

Response to Arguments

4. Applicant's arguments filed 1/30/04 have been fully considered but they are not persuasive for reasons as follow.

Applicant argues that Dawson et al. do not teach the claimed invention mainly because Dawson et al. do not teach forming initial single layer sidewall structure of similar widths adjacent to the NMOS transistor gate structure and the PMOS transistor gate structure.

In response to the argument, Dawson et al., in col. 6, lines 51-53, disclose that "another oxide layer .... is conformally deposited over the structure....." In other words, the another oxide layer, which acts as the initial single layer sidewall structure, covers the NMOS (126) and the PMOS (122) transistors including the sidewalls of (122) and (126), which can be reasonably and broadly interpreted as having similar-width oxide-sidewall-layer deposited adjacent to (122) and (126), because claim 1 does not expressly recite a processing step of how to form the "similar widths." In addition, the term "similar width " is so broad and not being well defined that the cited reference reads on it. For the above reason, the rejection, as set forth in the previous Office Action, is deemed proper.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Examiner
Art Unit 2823

April 17, 2004